ProDAQ

Hardware Manual

ProDAQ 3550

Fast DAC/AWG Function Card

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Bustec Production, Ltd.
World Aviation Park, Shannon, Co. Clare, Ireland
Tel: +353 (0) 61 707100, FAX: +353 (0) 61 707106

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Glossary

DAC	**D**igital-**A**nalog-**C**onverter
FC	**F**unction **C**ard
FCS	**F**unction **C**ard **S**pecific
FP	**F**ront **P**anel
MB	**M**other **B**oard
opt.	**opt**ional
ProDAQ	**Pro**fessional **D**ata **A**c**Q**uisition
RC	**R**ead only with **C**lear of status information after access
RCW	Read with **C**lear on status information, **W**rite
rec.	**rec**ommended
req.	**req**uired
res.	**res**erved
RO	**R**ead **O**nly
RWC	**R**ead, **W**rite with **C**lear on status information after access or after end of issued action
RW	**R**ead **W**rite operations
TRG	**TR**i**G**ger
VXI	**V**ME e**X**tension for **I**nstrumentation
WO	**W**rite **O**nly

1. Introduction

The ProDAQ 3550 Fast Digital-to-Analog Converter & Arbitrary Waveform Generator Function Card provides two channels per card, each equiped with a 16-bit, fast and precision Digital-to-Analog Converter, 2-pole analog filter and 256k x 16 SRAM memory per channel. Several standard output ranges as well as custom ones are available.

The ProDAQ 3550 can be used as a two-channel Waveform Generator. Two user defined waveforms, stored in two 256k x 16 SRAMs, can be created with an update time ranging from DC to 1 µs (1MHz). The memory can be divided into segments to store complex waveforms. Segments not currently used in a waveform can be loaded during running bursts providing higher data throughput. If a larger SRAM is required the ProDAQ 3550 can be configured as a single-channel, dual output DAC with 512k SRAM.

The ProDAQ 3550 function card is one of a range of function cards designed to provide full functionality when installed in one of the range of ProDAQ motherboard modules such as the ProDAQ 3120.

2. Installation

2.1 Unpacking and Inspection

The ProDAQ module is shipped in an antistatic package to prevent any damage from electrostatic discharge (ESD). Proper ESD handling procedures must always be used when packing, unpacking or installing any ProDAQ module, ProDAQ plug-in module or ProDAQ function card:

- Ground yourself via a grounding strap or similar, e.g. by holding to a grounded object.
- Discharge the package by touching it to a grounded object, e.g. a metal part of your VXIbus chassis, before removing the module from the package.
- Remove the ProDAQ module from its carton, preserving the factory packaging as much as possible.
- Inspect the ProDAQ module for any defect or damage. Immediately notify the carrier if any damage is apparent.

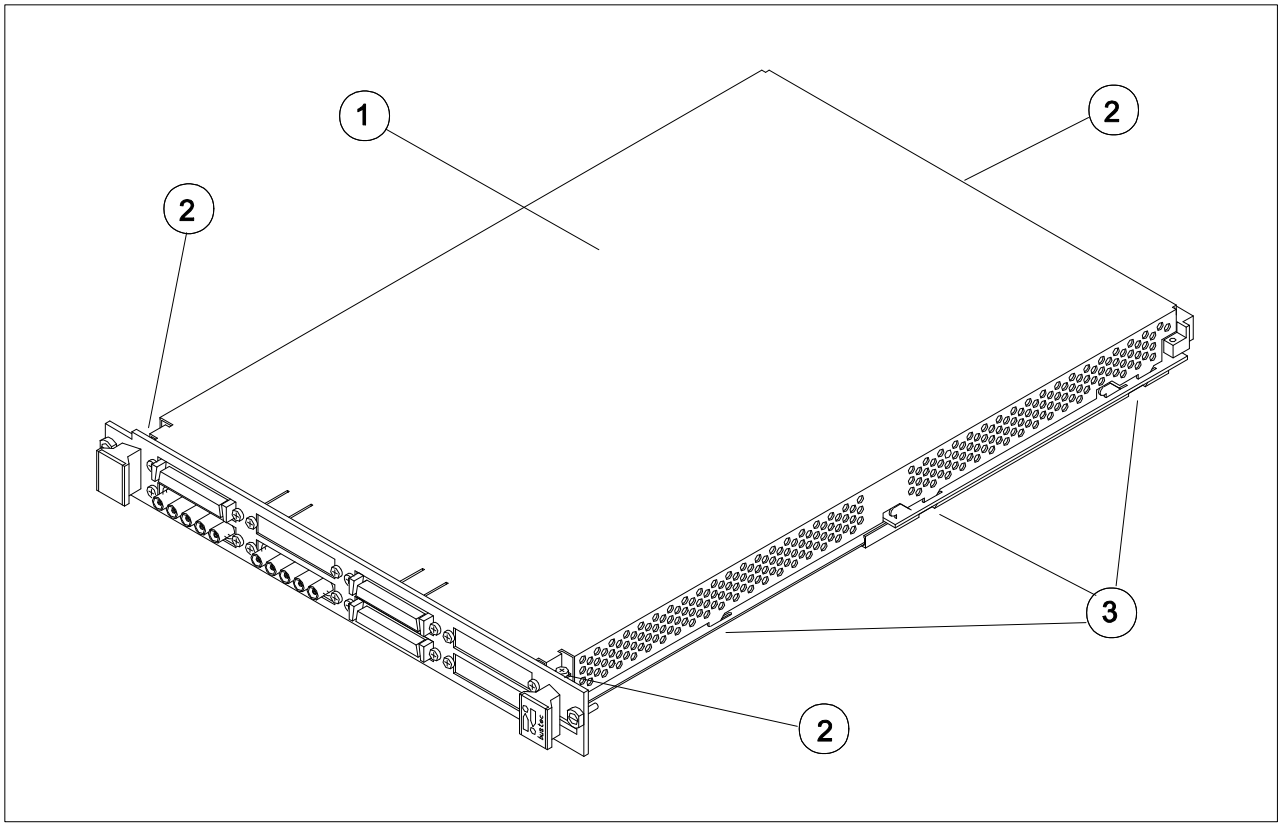
2.2 Reshipment Instructions

Use the original packing material when returning a ProDAQ module to Bustec Production Ltd. or calibration or servicing. The original shipping carton and the instrument's plastic foam will provide the necessary support for safe reshipment.

If the original anti-static packing material is unavailable, wrap the ProDAQ module in anti-static plastic sheeting and use plastic spray foam to surround and protect the instrument. Reship in either the original or a new shipping carton.

2.3 Preparing the ProDAQ Module

To install a ProDAQ Function Card into one of the ProDAQ Motherboards, you need to remove the modules top cover:



1 - Module Cover 2 - Cover Screws 3 - Cover Hooks

Figure 1 - Removing the ProDAQ Module Cover

To remove the top cover, remove the one countersunk screw in the back and the two panhead screws towards the front panel (②), that hold the cover in place. Remove the cover by sliding it out of its position towards the VXIbus connectors and up. Take special care about the hooks (③) holding it into place. Try not to lift the cover straight up. See Figure 1 for the location of the screws.

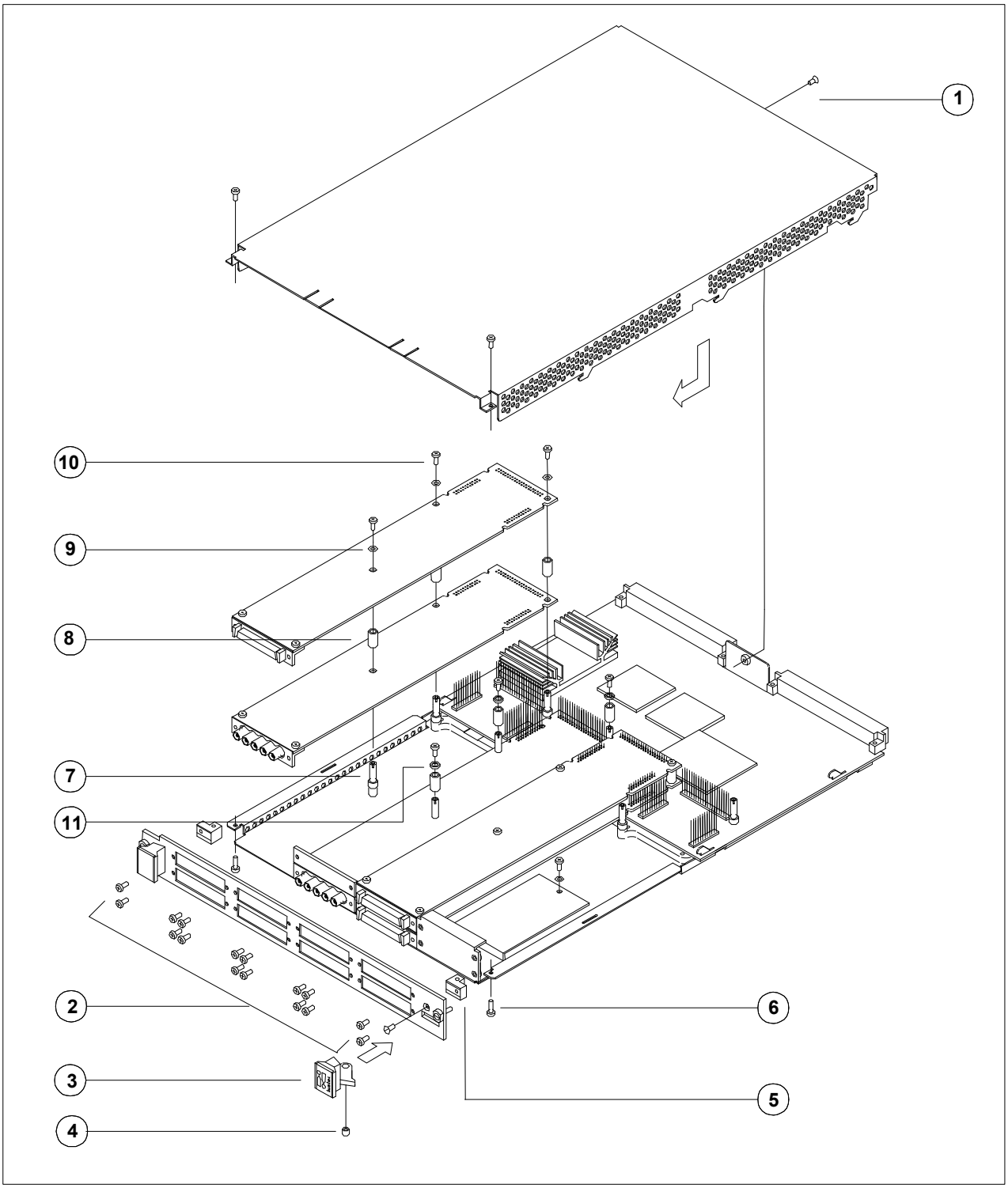
To re-install the cover, slide it back into its position by placing the small hooks over their holes and moving the cover down and forward. Secure the top cover using the two panhead screws and one countersunk screw (②).

2.4 Installing a ProDAQ Function Card

The ProDAQ Function Cards are arranged inside the ProDAQ Module in four stacks of two cards each. The function cards are mounted face down, e.g. the front-panel connectors as well as the motherboard connectors are underneath the PCB.

To install a ProDAQ Function Card in any of the possible positions, use the following procedure (See figure 2 for reference):

- Remove the top cover of the module as described earlier in this chapter (Fig. 2, Pos. 1).
- Remove all screws on the front-panel holding installed function cards or double filler panels in place (Fig. 2, Pos. 2). Screws holding single filler panels don't need to be removed.
- Remove the two panhead screws that mount the front panel to the modules bottom cover (Fig. 2, Pos. 6).
- Please take special care of the module handles and the rings (Fig. 2, Pos. 3 and 4), which are also fixed by those screws. The mounting angle (Fig. 2, Pos. 5) stays fixed to the front panel.
- Remove the front panel by moving it forward carefully so as to avoid bending the installed function cards.
- Choose the stack and position (lower or upper) where you want to mount the function card. If the stack, in which the function card should be installed, is covered by a double filler panel, you have to remove it before installing the function card.
- Remove the three 2.5mm panhead screws and the crinkle washers from the stack's standoffs (Fig. 2, Pos. 9 and 10 for example).
- If you want to install a function card in the upper position of a stack without having a function card in the lower position, you need to mount both spacers (Fig. 3, Pos. 11) on each standoff. If the stack is already populated with a function card in the lower position, mount only the bigger spacer (Fig. 2, Pos. 8) onto each standoff.
- Place a bayonet (supplied) on each standoff. Align the function card over these and slide carefully down. The function card should be held parallel to the modules bottom cover all the time during its way down.
- Fix the function card by mounting the three 2.5mm panhead screws and the crinkle washers onto each standoff. If you install a function card in the lower position of a stack, you need first to mount both spacers (Fig. 2, Pos. 11) onto each standoff.
- Re-mount the modules front-panel. If there is only one function card mounted in a stack, cover the remaining opening in the front panel by a single filler panel.
- Re-mount the modules top cover.



1 - 2.5mm Panhead Screws
2 - 2.5mm Panhead Screws
3 - Module Handle
4 - Ring
5 - Mounting Angle
6 - 2.5mm Panhead Screws
7 - Standoff
8 - Spacer
9 - Crinkle Washer
10 - 2.5mm Panhead Screw
11 - 2mm Spacer

Figure 2 - The ProDAQ Module Assembly

2.5 Removing a ProDAQ Function Card

Removing a ProDAQ Function Card is exactly the reverse operation then installing it. After removing the top cover and the front panel as described previously, remove the three roundhead screws that fix the function card(s) on the standoffs.

Take special care when removing the function card(s) not to bend the motherboard connectors.

After removing the function card(s), install the correct combination of spacers on the standoffs. If a stack is populated with only one function card, each of the standoffs needs to be mounted with both spacers to cover the distance between the cards as well as the PCB thickness of the missing card. If a stack is populated with two function cards, only the bigger spacer must be mounted.

Fix any remaining function card again by mounting the three panhead screws on the standoffs, re-mount the front panel and the modules cover.

3. Theory of Operation

The ProDAQ 3550 function card is a two-channel, fast and precision Digital-to-Analog Converter. Each channel contains a 256k x 16 SRAM, a 16-bit DAC, a 2-pole analog filter and an output buffer. Different output voltage options are available.

The ProDAQ 3550 can be used as a two-channel Waveform Generator. Two user defined waveforms, stored in two 256k x 16 SRAMs, can be created with an update time ranging from DC to 1µS (1MHz). The memory can be divided into segments to store complex waveforms. Segments not currently used in a waveform can be loaded during running bursts providing higher data throughput. If a larger SRAM is required the 3550 can be configured as a single-channel DAC with 512k SRAM.

Several trigger modes are available for synchronization purposes. Complex waveforms are accompanied with powerful trigger output signals to mark the events inside the waveforms.
The 2-pole analog filter (Sallen-Key type) provides three software-selectable cutoff frequencies. A filter bypass mode can also be selected. The output buffer provides necessary gain and output power. Software-controlled calibration automatically removes offset and gain errors providing unprecedented accuracy required for demanding DC and low frequency applications.

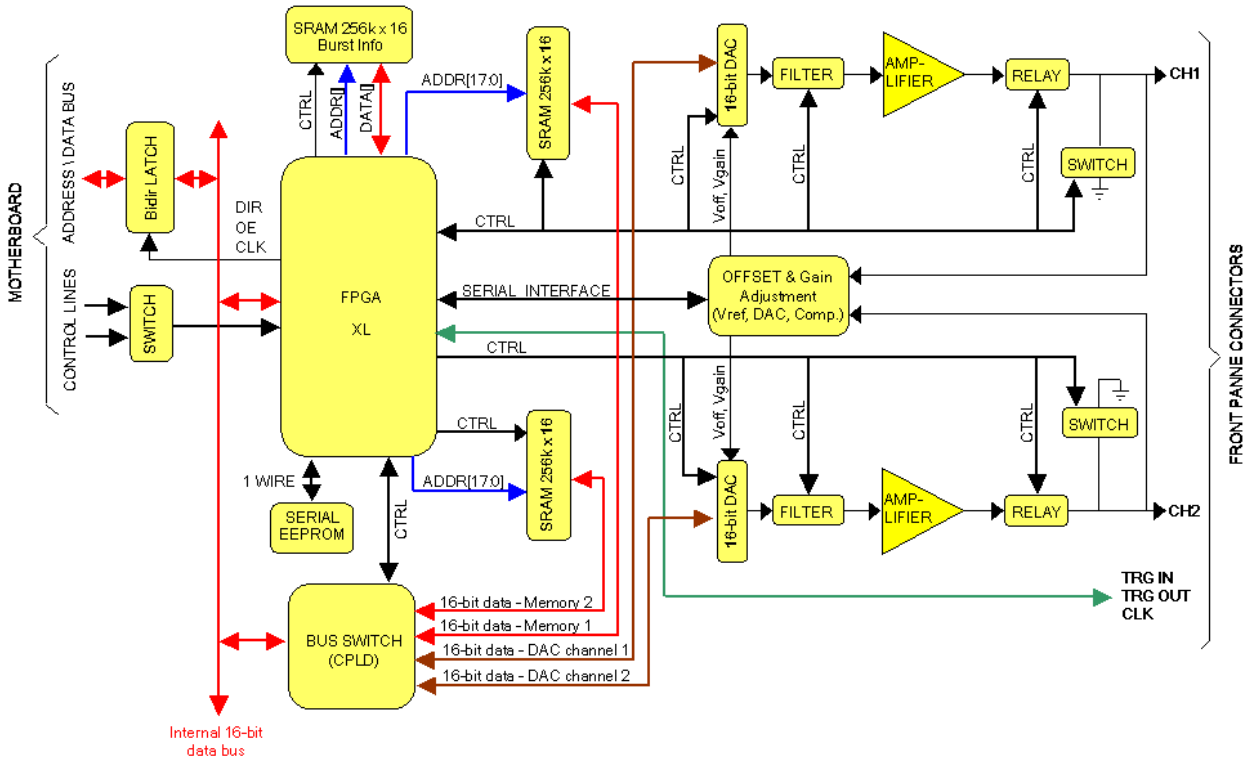


Fig. 1: ProDAQ 3550 Block Diagram

3.1 Operating Modes

3.1.1 Waveform / Burst Definition

3.1.1.1 Segment:

A segment is the basic element of a waveform and represents a certain signal that is to be generated by the DAC (e.g. one period of a sine wave). It can be defined from two points up to the full size of the memory (256k).
The memory can be divided into segments ranging from 1 up to 1024. The segments can be either of equal or different size. Note that the sum of points stored in all defined segments may not exceed the maximum size of the memory (256k).

Summary:

Segment Length – K_{SL}: $2 \leq K_{SL} \leq 256k$

Number of Segments – K_S: $1 \leq K_S \leq 1k$

3.1.1.1 Pattern:

A pattern is the sum of different segments. Up to 1024 segments can be included in a pattern. The minimum amount is two. If the number of segments in a pattern is equal to one the pattern is equivalent to the selected segment. It is possible to use one segment more than once inside a pattern.

Summary:

Pattern – P: $$P = \sum_{N=2}^{1024} SEG$$

3.1.1.2 Waveform:

The waveform is a multiple pattern; this means that the pattern can be repeated a specified number of times, defined by the waveform length. The waveform length can vary from two to 1024. The waveform is equivalent to the pattern if the waveform length is equal to one. The waveform length is common for both channels. A continuous mode is also available.

Summary:

Waveform Length – N_W: $2 \leq N_W \leq 1024$

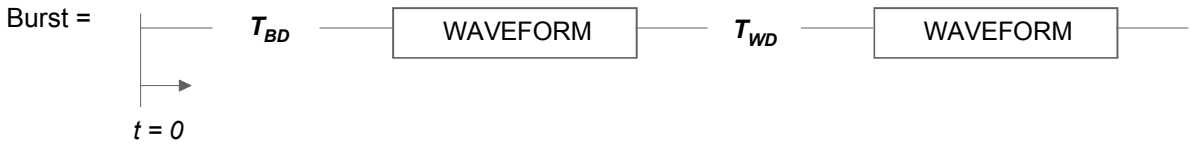
Waveform – W: $W = N_W * P$

3.1.1.3 Burst:

A burst is a sum of defined waveforms separated by a delay time, T_{WD}. The number of waveforms in the burst is defined by the burst size and can range from two up to 1024. A continuous mode is also available. The delay time between waveforms can range from 1µS to 1000S. If the burst size is equal to one the burst is equivalent to the waveform. A software command or an external trigger event can start a burst. The first segment of the burst is generated after the initial burst delay time, T_{BD} ranging from 100nS to 1000S.

Summary:

Burst Size – N_B:	$2 \leq N_B \leq 1024$
Burst Delay Time – T_{BD}:	$1\mu S \leq T_{BD} \leq 1000S$
Waveform Delay Time – T_{WD}:	$1\mu S \leq T_{WD} \leq 1000S$
Burst – B:	$B = \sum_{N_B} W$



3.1.2 Burst Operation

As mentioned above (see burst definition) software command or an external trigger event can start a burst.
The burst will be generated with the selected update time ranging from DC to 1µS (1MHz). The clock can be chosen from one of the following sources: the motherboard 40MHz-clock generator or the external clock supplied to the front panel connector.
To interrupt or stop a running burst especially in the continuous mode an external trigger event can be applied or a software command can be sent.
Summary:

Burst start:	software command, external Trigger from FP or MB
Burst stop:	software command, external Trigger from FP or MB
Burst mode:	single, continuous
Clock source:	MB, external Clock from FP
Output update time:	DC to 1µS (1MHz)

3.1.3 Trigger Output

Several events inside the burst can generate a trigger, which can be routed to the MB and/or the FP. The burst doesn't stop at these events. Normally the trigger output is a 100nS pulse. In case of the MB, the generation of a level can be selected. The active polarity of the trigger output signal is low for both the FP and the MB.

Following events are selectable:

- End of a segment, selectable for each segment
- End of the pattern
- End of the waveform
- Start of the burst
- End of the burst

3.1.4 Gate Mode

In the Gate Mode an external trigger signal can control the output channel. This signal works as a gate to inhibit the output signals. The trigger signal can come from either the FP and/or the MB.

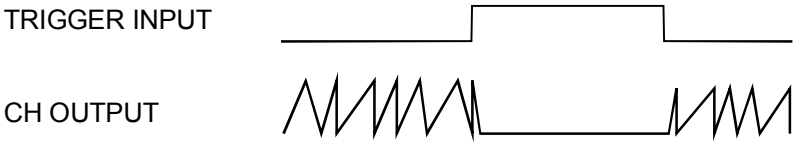


Fig. 2: Trigger input as gate signal

The following selections can be made:

- Channel1 gated & Channel2 not gated
- Channel1 not gated & Channel2 gated
- Both Channel1 & Channel2 gated

If the gate is asserted the burst operation reacts as follows. The burst operation will be stopped, the output signal will be inhibited and the burst operation will be resumed with the next sample after the gate signal is released.

4. Addresses and Registers

All registers appear as 16-bit registers on the internal data bus. From the VXIbus the registers have to be accessed as 16-bit registers aligned to a 32-bit border.

4.1 Address Map

All addresses are given in a hexadecimal notation.

VXI Address	Internal Address	Name	Access	Function
0	0	FCID	RO	ID register for automatic board identification
4	1	FCVER	RO	Version numbers
8	2	FCCSR	RCW	General control and status register
10	4	TrgInConf	RW	Trigger Input Configuration
14	5	TrgOutConf	RW	Trigger Output Configuration
18	6	SerPROM	RW	Read / write of serial PROM DS2430A and Subtype Version
1C	7	C1AddrHi	WO	Upper Address of Channel 1 Memory
20	8	C1AddrLo	WO	Lower Address of Channel 1 Memory
24	9	C2AddrHi	WO	Upper Address of Channel 2 Memory
28	A	C2AddrLo	WO	Lower Address of Channel 2 Memory
30	C	InfAddr	WO	Address of Burst Information Memory
34	D	TBD	RW	Burst Delay Time
38	E	UpdTime	RW	DAC Update Time
3C	F	TWD	RW	Waveform Delay Time
40	10	C1SegNo	RW	Number of Segments in Channel 1
44	11	C2SegNo	RW	Number of Segments in Channel 2
48	12	WaveLen	RW	Waveform Length
4C	13	BurstSize	RW	Burst Size
50	14	FilterSel	RW	Filter Selection
54	15	VoltRef	RW	Reference Voltages
58	16	Calib	RW	Channel Calibration
8000	2000	DAC1	RW	DAC channel 1 (through EPLD)
C000	3000	DAC2	RW	DAC channel 2 (through EPLD)
10000 – 17FFC	4000 - 5FFF	BurstInfo1	RW	Burst information memory for channel 1
18000 – 1FFFC	6000 - 7FFF	BurstInfo2	RW	Burst information memory for channel 2
20000 – 2FFFC	8000 - BFFF	BurstData1	RW	Output data memory for channel 1 (through EPLD)
30000 – 3FFFC	C000 - FFFF	BurstData2	RW	Output data memory for channel 2 (through EPLD)

4.2 Register Description

4.2.1 FCID

Location = 0x0

This register identifies the function card type and allows therefore the automatic board identification.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	1	1	0	1	0	1	0	1	0	1	0	0	0	0
Content	Function Card Type = 3550															

4.2.2 FCVER

Location = 0x1

This register contains the PCB version number and the FPGA version number.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	PCB Version								FPGA Version							

The subtype gives additional information about the function card type. It is stored in the Serial Prom (see 3.3.2.6)

4.2.3 FCCSR

Location = 0x2

This register provides the possibility to control the burst generation and delivers general states of the card.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	Burst Start	Soft Trig	Soft Abort	Soft Break	Ext Trig Enable	Ext Clk Enable	Cont Burst	Cont Wave	Sync Abort	Burst State	not used	Chan Mode	Mem Reload	Mem Extension	Chan 2	Chan 1

Burst Start: This bit prepares the internal logic for the burst operation and enables the burst start via Software or External Trigger. This bit has to be set until the burst generation is finished.

- one (1): burst operation enabled
- zero (0): burst operation disabled

The access to the following resources from the motherboard are disabled if the burst operation is enabled.

- C1AddrHi register
- C1AddrLo register
- C2AddrHi register
- C2AddrLo register
- InfAddr register
- TBD register
- UpdTime register
- TWD register
- DAC1 register
- DAC2 register
- Burst Information Memory

- Burst Data Memory 1, unless not used (free) in the reload mode
- Burst Data Memory 2, unless not used (free) in the reload mode

Soft Trig: Setting this bit starts the burst generation immediately. The bit will be cleared after the burst generation is finished.

- one (1): starts the burst generation (Software Trigger)
- zero (0): no action

Soft Abort: Setting this bit causes the abortion of the burst generation. Depending on the setting of the Sync Abort bit, the abortion happens either immediately or at the end of the current pattern. The bit will be cleared after the burst generation is finished.

- one (1): aborts the burst generation (Software Abort)
- zero (0): no action

Soft Break: Setting this bit stops the burst generation immediately. All current states will be kept. Resetting this bit resumes the burst generation with the next sample after the break.

- one (1): stops the burst generation (Software Break)
- zero (0): resumes the burst generation

Ext Trig Enable: Enables the start, stop and abort of the burst generation by an external trigger event. The source and the mode of the external trigger is defined in the Trigger Input Configuration register.

- one (1): External Trigger enabled
- zero (0): External Trigger disabled

Note: This setting does not affect the possibility to control the burst generation by the software commands (Soft Trig, Soft Break and Soft Abort).

Ext Clk Enable: This bit specifies whether the programmable clock circuitry (TBD, UpdTime, TWD) operates with the internal base clock or an external clock supplied to the FP.

- one (1): External Clock selected
- zero (0): Internal Base Clock selected

Cont Burst: Selects the continuous burst generation. If not selected, the burst generation stops after completion of the numbers of waveforms given in the BurstSize register.

- one (1): Continuous burst enabled
- zero (0): Continuous burst disabled

Cont Wave: Selects the continuous waveform generation. If not selected, the waveform generation stops after completion of the number of patterns given in the WaveLen register.

- one (1): Continuous waveform enabled
- zero (0): Continuous waveform disabled

Sync Abort: Selects the synchronous abortion mode of the burst generation. If enabled, the burst generation stops at the end of the current pattern, when a Software Abort command or an External Trigger occurs.

- one (1): Synchronous Abort enabled
- zero (0): Synchronous Abort disabled

Burst State: Reading this bit returns the state of the burst generation. The Burst State is read-only.

- one (1): burst generation is in progress
- zero (0): burst generation is finished or not started yet (triggered)

Chan Mode: Defines the mode for direct accesses to the DAC registers from the motherboard. There is an independent DAC update mode for both channels and a synchronous DAC update mode, which allows the update of both channels synchronously.

In the case of the **independent mode**, the DAC (either channel 1 or 2) will be updated after a write access to the corresponding DAC register.

In the **synchronous mode**, both DACs (channel 1 and 2) will be updated synchronously after a write access to the DAC2 register (channel 2).

- ❑ one (1): dependent (synchronous) mode
- ❑ zero (0): independent mode

Mem Reload: Selects the reload mode**,** which allows reloading data to one memory segment (physical memory) while the other memory segment is used to generate the samples. This option is available for either only one channel or both channels simultaneously. If the memory reload mode is active, the continuous waveform mode has to be selected.

- ❑ one (1): Memory reload is enabled
- ❑ zero (0): Memory reload is disabled

Mem Extension: Extends the Burst Data Memory for the selected channel from max. 256K to max. 512K. This option is not available if Mem Reload is active or both channels are enabled.

- ❑ one (1): Memory extension is enabled
- ❑ zero (0): Memory extension is disabled

Chan 2: Selects channel 2 for the waveform generation.

- ❑ one (1): Channel 2 is enabled
- ❑ zero (0): Channel 2 is disabled

Chan 1: Selects channel 1 for the waveform generation.

- ❑ one (1): Channel 1 is enabled
- ❑ zero (0): Channel 1 is disabled

4.2.4 TrgInConf

Location = 0x4

This register defines the trigger input configuration. The settings in this register control the burst if external trigger is enabled.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	x	x	x	x	0	0	0	0	x	x
Content	not used										FP In En	MB In En	Mode	Sub Mode	not used	

FP In En: Controls the Front Panel trigger input.

- ❑ one (1): input enabled
- ❑ zero (0): input disabled

MB In En: Controls the trigger input from the motherboard.

- ❑ one (1): input enabled
- ❑ zero (0): input disabled

Mode / Sub Mode: Specifies the mode for external input trigger and how the burst generation reacts.

Mode	Sub Mode	Name	Description
0	0	Pulse / Abort	1. The first falling edge on an external trigger line starts the burst generation 2. The next falling edge aborts the burst generation if the burst is still running
0	1	Pulse / Break	1. The first falling edge on an external trigger line starts the burst generation 2. The next falling edge works as burst break if the burst is still running 3. The burst generation will be resumed with the next falling edge after the burst break 4. Steps 2 & 3 can be repeated until the burst end is reached
1	x	Gate	1. The burst starts with a low level on an external trigger line after the burst generation has been enabled 2. The burst generation keeps running as long as the level on the external trigger stays low 3. If the external trigger goes high, then the burst generation breaks, the output of the channel keeps the last value 4. The burst resumes when the trigger goes low again 5. Steps 3 & 4 can be repeated until the burst end is reached

Note: For more details of the modes see 3.4.3.7 Burst Control by External Trigger

4.2.5 TrgOutConf

Location = 0x5

This register defines the trigger output configuration. The settings in this register control the generation of trigger events.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	TrgOut State	Error State	SigOut Enable	MemSeg 2 State	MemSeg 1 State	not used	not used	not used	FP Out En	MB Out Type	MB Out En	Start Burst En	End Burst En	End Wave En	End Patt En	End Seg En

TrgOut State: Reading this bit returns the state of the trigger output line to the motherboard.

- one (1): trigger output line is asserted
- zero (0): trigger output line is not asserted

Error State: Reading this bit returns the state of the error line to the motherboard. Since the error line is not used, the Error State is always zero (not asserted).

SigOut Enable: Enables the output driver of the dedicated signal line to the motherboard. This line is used to announce special events.

- one (1): output driver enabled
- zero (0): output driver disabled

MemSeg 2 State: Returns the state of the Data Memory 2 in the online Reload mode.

- one (1): memory is free to be reloaded
- zero (0): memory is in use for the sample generation

MemSeg 1 State: Returns the state of the Data Memory 1 in the online Reload mode.

- one (1): memory is free to be reloaded
- zero (0): memory is in use for the sample generation

FP Out En: Controls the Front Panel trigger output.

- one (1): output enabled
- zero (0): output disabled

MB Out Type: Defines the type of the trigger signal to be sent to the motherboard.

- one (1): Pulse, 100ns width, active low
- zero (0): Level, active low

MB Out En: Controls the trigger output to the motherboard.

- one (1): output enabled
- zero (0): output disabled

Start Burst En: Enables the burst start for trigger event generation

- one (1): burst start for trigger enabled
- zero (0): burst start for trigger disabled

End Burst En: Enables the burst end for trigger event generation

- one (1): burst end for trigger enabled
- zero (0): burst end for trigger disabled

End Wave En: Enables the waveform end for trigger event generation

- one (1): waveform end for trigger enabled
- zero (0): waveform end for trigger disabled

End Patt En: Enables the pattern end for trigger event generation

- one (1): pattern end for trigger enabled
- zero (0): pattern end for trigger disabled

End Seg En: Enables the segment end for trigger event generation

- one (1): segment end for trigger enabled
- zero (0): segment end for trigger disabled

Note: There is an additional enable bit for each segment in the Burst Information Memory.

4.2.6 SerPROM

4.2.6.1 Register Description

Location = 0x6

Using this register data can be written to or read from the on-board serial EEPROM (type Dallas DS2430A).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0
Content (write)	not used					Command			Data							
						Reset	Write	Read								
Content (read)	not used						FSM ready	PROM present	Data							

Command: The command bits specify the action the PROM interface logic shall do. The information will be cleared after the execution of the command has been finished.

- Reset: Writing a one initiates the PROM's reset. This command is necessary after the completion of a read or write access to one of the PROM's memory areas. For detailed information see data sheet Dallas DS2430A.
  Writing a zero to this bit has no effect.
- Write: Writing a one to this bit initiates the transfer of the byte specified in the Data field to the PROM. The data can represent data, address or command bits. For detailed information see data sheet Dallas DS2430A.
  Writing a zero to this bit has no effect.
- Read: Writing a one to this bit initiates a read of one data byte from the PROM. The software can read this data from the Data field. For detailed information see data sheet Dallas DS2430A.
  Writing a zero to this bit has no effect.

PROM present: This information is used during the execution of a Reset command. A one read from this bit indicates that the PROM is present and able to react on further actions.

FSM ready: This bit indicates the state of the command execution. A one means the PROM interface is ready to process a new command. A zero means that the execution is still in progress and further commands will be ignored.

Data: This byte specifies the data that has to be transferred to the PROM using a Write command. When read this field represents the last data read from the PROM.

4.2.6.2 FDAC Subtype

The serial PROM stores the FDAC subtype. The subtype gives additional information about the function card type, which might be necessary for using the right device driver.

The following are the 12 different types of FDAC.

Subtype (hex)	FDAC type
AA	+5V
AB	+10V
AC	+20V
BA	± 5V
BB	± 10V
BC	± 20V

The subtype is read from Address = 0 of the Serial PROM (location = 0x6).

4.2.7 C1AddrHi

Location = 0x7

This register contains the upper 2-bits of the address for accesses to the memory storing the data of channel 1 (Data Memory 1).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0
Content	not used														Addr high	

Addr high: Defines the bits 17 to 16 of the base address for accesses to the Burst Data Memory of channel 1.

4.2.8 C1AddrLo

Location = 0x8

This register contains the lower 16-bits of the address for accesses to the memory storing the data of channel 1 (Data Memory 1). **Note:** Addr low has to be set before Addr high.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	Addr low															

Addr low: Defines the bits 15 to 0 of the base address for accesses to the Burst Data Memory of channel 1.

4.2.9 C2AddrHi

Location = 0x9

This register contains the upper 2-bits of the address for accesses to the memory storing the data of channel 2 (Data Memory 2).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	X	x	x	x	x	x	x	x	x	x	x	0	0
Content	not used														Addr high	

Addr high: Defines the bits 17 to 16 of the base address for accesses to the Burst Data Memory of channel 2.

4.2.10 C2AddrLo

Location = 0xA

This register contains the lower 16-bits of the address for accesses to the memory storing the data of channel 2 (Data Memory 2).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	Addr low															

Addr low: Defines the bits 15 to 0 of the base address for accesses to the Burst Data Memory of channel 2.

Note: Addr low has to be set before Addr high.

4.2.11 InfoMemAddr

Location = 0xC

This register contains the address for accesses to the memory storing the burst information data. This register is used to define the address for the Burst Information Memory of channel 1 and channel 2.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0
Content	not used				Addr											

Addr: Defines the base addresses for accesses to the Burst Information Memory of channel 1 and channel 2.

4.2.12 TBD

Location = 0xD

This register contains the initial Burst Delay Time and specifies the time between a burst start and the first value will be written to the DAC. A time base multiplied by the time value calculates the time.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	not used			Time Base			Time Value									

Time Base: The time base gives the range as well as the step size of the Burst Delay Time. There are eight different ranges available.

Internal Base Clock:

Content	Time Base	Range	Accuracy
000	100ns	1µs … 100µs	+50ns
001	1µs	1µs … 1ms	+50ns
010	10µs	10µs … 10ms	+100ns
011	100µs	100µs … 100ms	+150ns
100	1ms	1ms … 1s	+200ns
101	10ms	10ms … 10s	+250ns
110	100ms	100ms … 100s	+300ns
111	1s	1s … 1000s	+350ns

Note: Due to the maximum update frequency of the used DAC, the first range starts only at 1µs.

External Clock (ExtClk):

Content	Time Base	Accuracy
000	ExtClk	+50ns
001	ExtClk / 10	+50ns
010	ExtClk / 100	+100ns
011	ExtClk / 1000	+150ns
100	ExtClk / 10^4	+200ns
101	ExtClk / 10^5	+250ns
110	ExtClk / 10^6	+300ns
111	ExtClk / 10^7	+350ns

Note: The maximum frequency of the external clock is 20MHz and the resulting delay time must not be lower than 2µs.

Time Value: The time value determines the number of counts in a certain range specified by the time base. The resulting Burst Delay Time can be calculated in the following way.

*Burst Delay Time = Time Base * Time Value + Accuracy*

Clock Source	Minimum Burst Delay Time
Internal Base Clock	1µs
External Clock	2µs

Example (internal base clock):

Time Base Content	Time Value Content	Burst Delay Time
001	0x80	1µs * 128 + 50ns = 128.05µs

4.2.13 UPDTIME

Location = 0xE

This register contains the initial Update Time and specifies the time between two values written to the DAC. A time base multiplied by the time value calculates the time.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	not used			Time Base			Time Value									

Time Base: The time base gives the range as well as the step size of the Update Time. There are eight different ranges available.

Internal Base Clock:

Content	Time Base	Range			Accuracy
000	100ns	1µs	…	100µs	+50ns
001	1µs	1µs	…	1ms	+50ns
010	10µs	10µs	…	10ms	+100ns
011	100µs	100µs	…	100ms	+150ns
100	1ms	1ms	…	1s	+200ns
101	10ms	10ms	…	10s	+250ns
110	100ms	100ms	…	100s	+300ns
111	1s	1s	…	1000s	+350ns

Note: Due to the maximum update frequency of the used DAC, the first range starts only at 1µs.

External Clock (ExtClk):

Content	Time Base	Accuracy
000	ExtClk	+50ns
001	ExtClk / 10	+50ns
010	ExtClk / 100	+100ns
011	ExtClk / 1000	+150ns
100	ExtClk / 10^4	+200ns
101	ExtClk / 10^5	+250ns
110	ExtClk / 10^6	+300ns
111	ExtClk / 10^7	+350ns

Note: The maximum frequency of the external clock is 20MHz and the resulting update time must not be lower than 1µs.

Time Value: The time value determines the number of counts in a certain range specified by the time base. The resulting Update Time can be calculated in the following way.

*Update Time = Time Base * Time Value + Accuracy*

Clock Source	Minimum Update Time
Internal Base Clock	1µs
External Clock	1µs

Example (internal base clock):

Time Base Content	Time Value Content	Update Time
000	0xA	100ns * 10 + 50ns = 1.05µs (minimum update time)

4.2.14 TWD

Location = 0xF

This register contains the Waveform Delay Time and specifies the time between two waveforms. A time base multiplied by the time value calculates the time.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	not used			Time Base			Time Value									

Time Base: The time base gives the range as well as the step size of the Waveform Delay Time. There are eight different ranges available.

Internal Base Clock:

Content	Time Base	Range	Accuracy
000	100ns	1µs … 100µs	+50ns
001	1µs	1µs … 1ms	+50ns
010	10µs	10µs … 10ms	+100ns
011	100µs	100µvs … 100ms	+150ns
100	1ms	1ms … 1s	+200ns
101	10ms	10ms … 10s	+250ns
110	100ms	100ms … 100s	+300ns
111	1s	1s … 1000s	+350ns

Note: Due to the maximum update frequency of the used DAC, the first range starts only at 1µs.

External Clock (ExtClk):

Content	Time Base	Accuracy
000	ExtClk	+50ns
001	ExtClk / 10	+50ns
010	ExtClk / 100	+100ns
011	ExtClk / 1000	+150ns
100	ExtClk / 10^4	+200ns
101	ExtClk / 10^5	+250ns
110	ExtClk / 10^6	+300ns
111	ExtClk / 10^7	+350ns

Note: The maximum frequency of the external clock is 20MHz and the resulting delay time must not be lower than 1µs.

Time Value: The time value determines the number of counts in a certain range specified by the time base. The resulting Waveform Delay Time can be calculated in the following way.

*Waveform Delay Time = Time Base * Time Value + Accuracy*

Clock Source	Minimum Burst Delay Time
Internal Base Clock	1µs
External Clock	1µs

Example (internal base clock):

Time Base Content	Time Value Content	Waveform Delay Time
100	0x3AF	1ms * 943 + 200ns = 0.9430002s

4.2.14.1 C1SegNo

Location = 0x10

This register defines the number of segments included in the pattern for channel 1 (Data Memory 1).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Content	not used						Segment No									

Segment No: Specifies how many segments are included in the pattern.

Segment No.	Number of Segments
0	1
1	2
…	…
1023	1024

4.2.15 C2SegNo

Location = 0x11

This register defines the number of segments included in the pattern for channel 2

(Data Memory 2).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Content	not used						Segment No									

Segment No: Specifies how many segments are included in the pattern.

	Number of Segments
0	1
1	2
…	…
1023	1024

4.2.16 WaveLen

Location = 0x12

This register defines the waveform length.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Content	not used						Wavelength									

Wavelength: Specifies the number of repetitions of pattern. This value is not valid if the waveform is configured in the continuous mode. This value is common to both channels.

Wavelength	Number of Repetition
0	0
1	1
…	…
1023	1023

4.2.17 BurstSize

Location = 0x13

This register defines the size of the burst.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Content	not used						Burstsize									

Burstsize: Specifies the number of repetitions of waveforms. This value is not valid if the burst is configured in the continuous mode.

Burstsize	Number of Repetition
0	0
1	1
…	…
1023	1023

4.2.18 FilterSel

Location = 0x14

This register allows the selection of the filter characteristic of both channels.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	x	x	1	1	x	x	1	1	x	x	1	1	x	x	1	1
Content	not used		Ch2 GNDlow	Ch2 RELlow	not used		Filter Ch2		not used		Ch1 GNDlow	Ch1 RELlow	not used		Filter Ch1	

Filter Ch2: Sets the filter characteristic of channel 2.

Value	Characteristic
00	1kHz cutoff frequency
01	10kHz cutoff frequency
10	100kHz cutoff frequency
11	Bypass

Ch2 RELlow: Controls the output relay of Ch2.

- one (1): Relay open
- zero (0): Relay closed

Ch2 GNDlow: Controls the switch to GND on the output of Ch2. Setting this bit to 1 when Ch2 RELlow is 0 doesn't ground the output.

- one (1): Output not grounded
- zero (0): Output grounded

Filter Ch1: Sets the filter characteristic of channel 1.

Value	Characteristic
00	1kHz cutoff frequency
01	10kHz cutoff frequency
10	100kHz cutoff frequency
11	Bypass

Ch1 RELlow: Controls the output relay of Ch1.

- one (1): Relay open
- zero (0): Relay closed

Ch1 GNDlow: Controls the switch to GND on the output of Ch1. Setting this bit to 1 when Ch1 RELlow is 0 doesn't ground the output.

- one (1): Output not grounded
- zero (0): Output grounded

4.2.19 VoltRef

Location = 0x15

To adjust the reference voltages for the automatic calibration process this register has to be used. Any write access to this register starts the setting!

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	Start	Busy	not used	Select	Vref value											

Start / Busy: The combination of these two bits indicates the state of the setting process. The software can use it to determine whether the action is finished and a new adjustment can be performed.

Start	Busy	Action State
0	0	The internal logic is ready to accept a new setting request.
1	0	A setting request has been sent by software, but the execution has not been started yet. Further writes will be ignored in this state.
1	1	The setting process is in progress. Further writes will be ignored in this state.

Select: This bit specifies the reference voltage circuitry that has to be adjusted.

- one (1): negative reference voltage
- zero (0): positive reference voltage

Vref value: This is the value to be written to the serial DAC to adjust the selected reference voltage circuitry. After the first adjustment this value is stored in the DS2430 PROM. The reference voltage has to be adjusted after each power-on. For this the driver has to read the value from the PROM and to write it to this register. The transfer to the serial DAC will be performed automatically.

4.2.20 Calib

Location = 0x16

The FDAC function card has automatic calibration circuitry for offset and gain adjustment. To perform the calibration this register has to be used. Any write access to this register starts the calibration process!

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content (write)	not used						Calib type	FC type	not used	Source			not used			
Content (read)	Start	Busy	Comp (FF)	Comp	Calib Value											

Start / Busy: The combination of these two bits indicates the state of the calibration process The software can use it to determine whether the calibration is finished and a new calibration can be performed.

Start	Busy	Action State
0	0	The internal logic is ready to accept a new calibration request.
1	0	A calibration request has been sent by software, but the execution has not been started yet. Further writes will be ignored in this state.
1	1	The calibration process is in progress. Further writes will be ignored in this state.

Comp (FF): Reading this bit, a one indicates the voltage of the selected source is higher than the reference voltage. A zero indicates the voltage is lower than the reference. The value is only valid after the calibration process is finished.

Comp: Reading this bit, a one indicates the voltage of the selected source is higher than the reference voltage. A zero indicates the voltage is lower than the reference. The value reflects the state of the comparator output.

Calib type: This bit specifies, which voltage has to be adjusted, either offset or gain.

Value	Type
0	offset adjustment
1	gain adjustment

The offset adjustment has to be performed always before gain adjustment.

FC type: The different types of Function Cards need a slightly different calibration approach. This field denotes the function card type.

Value	Type
0	unipolar, positive output voltage range or bipolar
1	unipolar, negative output voltage range

Source: The source field is used to select the channel for calibration.

Value	Source
0xx	not used
100	channel 1
101	channel 2
11x	not used

When performing a calibration the filter, output relay and switch settings can be set using the FilterSel register. See 3.3.2.19 FilterSel.

4.2.21 DAC1

Location = 0x2000

This 16-bit register allows the direct access from the motherboard to the 16-bit Digital to Analog Converter (DAC) of channel 1. The register is located in the EPLD and can be read from or written to. After a new value has been written to this location, the on-board logic transfers the value to the DAC automatically. This action can be synchronized with the update of channel 2 (see Chan Mode in the FCCSR register).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	DAC Value															

DAC Value: The DAC value depends on the Function Card subtype.

Subtype	neg. full-scale	neg. half-scale	zero	pos. half-scale	pos. full-scale
unipolar, positive	NA	NA	8000h	0h	7FFFh
unipolar, negative	7FFFh	0h	8000h	NA	NA
bipolar	8000h	C000h	0h	4000h	7FFFh

4.2.22 DAC2

Location = 0x3000

This 16-bit register allows the direct access from the motherboard to the 16-bit Digital to Analog Converter (DAC) of channel 2. The register is located in the EPLD and can be read from and written to. After a new value has been written to this location, the on-board logic transfers the value to the DAC automatically. This action can be synchronized with the update of channel 1 (see Chan Mode in the FCCSR register).

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Content	DAC Value															

DAC Value: The DAC value depends on the Function Card subtype.

Subtype	neg. full-scale	neg. half-scale	zero	pos. half-scale	pos. full-scale
unipolar, positive	NA	NA	8000h	0h	7FFFh
unipolar, negative	7FFFh	0h	8000h	NA	NA
bipolar	8000h	C000h	0h	4000h	7FFFh

4.2.23 BurstInfo1

Location = 0x4000 – 0x5FFF

This area of 8k addresses provides a window for accesses from the motherboard to the Burst Information memory of channel 1 (Data Burst Memory 1). Data can be read or written using single or block transfers.

Despite the possibility to access the memory through each address in the window, there is no relation between the window address and the real memory address. The InfoMemAddr register specifies the memory address. The memory address will be increased after each data value read or written to the memory.

The access to the memory is prohibited when the burst generation is enabled (FCCSR / Burst Start).

For the data structure of the Burst Information memory see chapter 3.4.2.

4.2.24 BurstInfo2

Location = 0x6000 – 0x7FFF

This area of 8k addresses provides a window for accesses from the motherboard to the Burst Information memory of channel 2 (Burst Data Memory 2). Data can be read or written using single or block transfers.

Despite the possibility to access the memory trough each address in the window, there is no relation between the window address and the real memory address. The InfoMemAddr register specifies the memory address. The memory address will be increased after each data value read or written to the memory.

The access to the memory is prohibited when the burst generation is enabled (FCCSR / Burst Start).

For the data structure of the Burst Information memory see chapter 3.4.2.

4.2.25 BurstData1

Location = 0x8000 – 0xBFFF

This area of 16k addresses provides a window for accesses to the Burst Data memory of channel 1 (Burst Data Memory 1). Data can be read or written using single or block transfers.

Despite the possibility to access the memory trough each address in the window, there is no relation between the window address and the real memory address. The C1AddrLo and C1AddrHi registers specify the memory address. The memory address will be increased after each data value read or written to the memory.

Note: For changing the memory address, the C1AddrLo register has to be set before setting the C1AddrHi register.

The access to the memory is prohibited when the burst generation is enabled (FCCSR / Burst Start), unless the Reload Mode is selected and the memory is not in use to generate samples. To check if the access is allowed read MemSeg 1 State in the TrgOutConf register.

For the data structure of the Burst Data memory see chapter 3.4.1.

4.2.26 BurstData2

Location = 0xC000 – 0xFFFF

This area of 16k addresses provides a window for accesses to the Burst Data memory of channel 2 (Data Burst Memory 2). Data can be read or written using single or block transfers.

Despite the possibility to access the memory trough each address in the window, there is no relation between the window address and the real memory address. The C2AddrLo and C2AddrHi registers specify the memory address. The memory address will be increased after each data value read or written to the memory.

Note: For changing the memory address, the C2AddrLo register has to be set before setting the C2AddrHi register.

The access to the memory is prohibited when the burst generation is enabled (FCCSR / Burst Start), unless the Reload Mode is selected and the memory is not in use to generate samples. To check if the access is allowed read MemSeg 2 State in the TrgOutConf register.

For the data structure of the Burst Data memory see chapter 3.4.1.

5. Detailed Description

5.1 Burst Data Memory

The Burst Data memory contains the 16-bit values (DAC Value) to be applied to the DAC during a running burst. Each channel is equipped with its own 256k*16-bit SRAM.

The memory can be divided into segments as described in 3.2.1. Waveform / Burst Definition. The start addresses, length and the order of segments are defined by the information in the Burst Information Memory. The data (DAC Values) within a segment are stored in an ascending order.

There is the possibility to extend the memory for one channel up to 512k*16-bit by using the memory of the other channel. Furthermore, a so-called online reload mode can be used to generate waveforms of unlimited length. For more information about the usage of the Burst Data Memory in the different modes see 3.4.3 Burst Operating Modes.

5.2 Burst Information Memory

Each Burst Data Memory has a Burst Information Memory of 4k*16-bit that stores additional information about the segmentation of the Burst Data Memory. This information is requested by the hardware for generating complex waveforms.

The information for the first segment in a pattern, waveform or burst always starts at address zero (0) of the Burst Information Memory. The information is stored in an ascending order and takes 3 addresses for each segment. The order of the segments described in the Burst Information Memory determines the order of the segments in the pattern, waveform or burst.

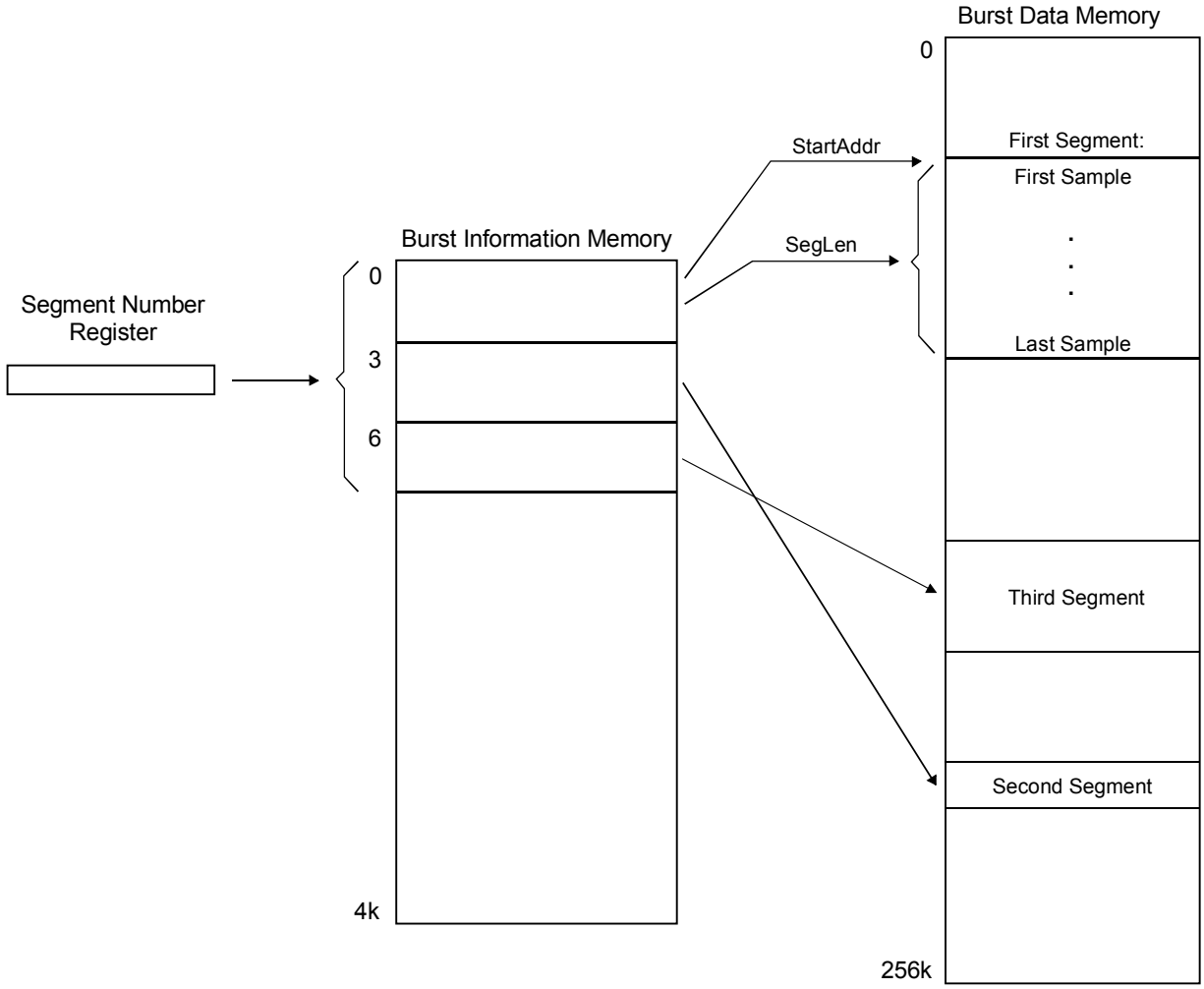
The number of segments used in the burst and described in the Burst Information Memory is given in the Segment Number register. This is either C1SegNo for BurstInfo1 or C2SegNo for BurstInfo2.

The structure of the information for one segment in the Burst Information Memory is as follows.

StartAddrLo:	Lower part of the start address of the segment (bits 15:0)
StartAddrHi:	Upper part of the start address of the segment (bits 17:16)
SegLenLo:	Lower part of the segment length (bits 15:0)
SegLenHi:	Upper part of the segment length (bits 17:16)
TrgEn:	Enables the trigger event generation at the end of the segment

- one (1): trigger enabled
- zero (0): trigger disabled

The relation between the Segment Number register, the Burst Information Memory and the Burst Data Memory is shown in the following figure.



5.3 Burst Operating Modes

5.3.1 Normal Mode

In the Normal Mode, there is one Burst Data Memory including the corresponding Burst Information Memory assigned to each of the two channels.

Channel	Burst Data Memory	Burst Information Memory	Segment Number Register	Maximum Number of Segments	Maximum Numbers of Samples
1	BurstData1	BurstInfo1	C1SegNo	1024	256k
2	BurstData2	BurstInfo2	C2SegNo	1024	256k

The burst generation can be started with either only Channel 1 active, only Channel 2 active or both channels active. The burst will be generated with the programmed Burst Delay Time (TBD), Update Time (UpdTime) and Waveform Delay Time (TWD). These times are common to both channels. The Normal Mode is selected when the Mem Extension and the Mem Reload bits in the FCCSR register are not set.

5.3.2 Memory Extension Mode

The Memory Extension Mode can be used only with one channel active. The Burst Data Memory of the other (inactive) channel is used in addition to the own memory to define waveforms with up to 512k different samples.
The burst starts always with Burst Data Memory 1 and switches to Burst Data Memory 2 when all segments defined in Burst Data Memory 1 are finished. This is independent of the selected channel.

Execution Order	Burst Data Memory	Burst Information Memory	Segment Number Register	Maximum Number of Segments	Maximal Numbers of Samples
1.	BurstData1	BurstInfo1	C1SegNo	1024	256k
2.	BurstData2	BurstInfo2	C2SegNo	1024	256k

The minimum total number of segments in the Extension Mode is two, one segment for each Burst Data Memory. A segment can not cross the physical border between the two Burst Data Memories. Programmable clock, continuous waveform, burst, external clock and trigger are available in this mode.
Set the Mem Extension bit in the FCCSR register to select the Memory Extension Mode. There is no automatic prevention if the Extension Mode, the Reload Mode or both channels are selected at the same time. Therefore, the resulting waveform is unknown.

5.3.3 Online Memory Reload Mode

The Online Memory Reload Mode provides the possibility to generate waveforms of unlimited length. The internal circuitry uses one Burst Data Memory to generate the samples while the software can write new data to the other Burst Data Memory. As in the Memory Extension Mode, the burst always starts with Burst Data Memory 1 and switches to Burst Data Memory 2. Since the Reload Mode is a continuous waveform mode, the burst generation switches back to Burst Data Memory 1 after Burst Data Memory 2.
The state of the Burst Data Memories can be checked by reading the Memory Segment State bits in the TrgOutConf register.

Memory Segment State		State Description
MemSeg 2 State	MemSeg 1 State	
1	0	Burst Data Memory 1 in use for sample generation, motherboard access disabled Burst Data Memory 2 enabled for reload
0	1	Burst Data Memory 2 in use for sample generation, motherboard access disabled Burst Data Memory 1 enabled for reload

In addition to the state bits, the circuitry generates a pulse on the Signal line (SIGlow or SIGup / FC interface) at each switch from one Burst Data Memory to the other Burst Data Memory. The pulse has a width of 50ns and can be used as an interrupt to announce that new data can be reloaded. The output driver of the Signal line has to be enabled by setting the SigOut Enable bit in the TrgOutConf register.

The Memory Reload Mode can be used with either only Channel 1 active, only Channel 2 active or both channels active. The data in the Burst Data Memory are multiplexed when both channels are active (see Data Structure / Memory Segmentation).

Set the Mem Reload bit in the FCCSR register to select the Online Memory Reload Mode. There is no automatic prevention if the Extension Mode and the Reload Mode are selected at the same time. Therefore, the resulting waveform is unknown. The Cont Wave bit in the FCCSR register has to be set for proper functioning of the Reload mode.

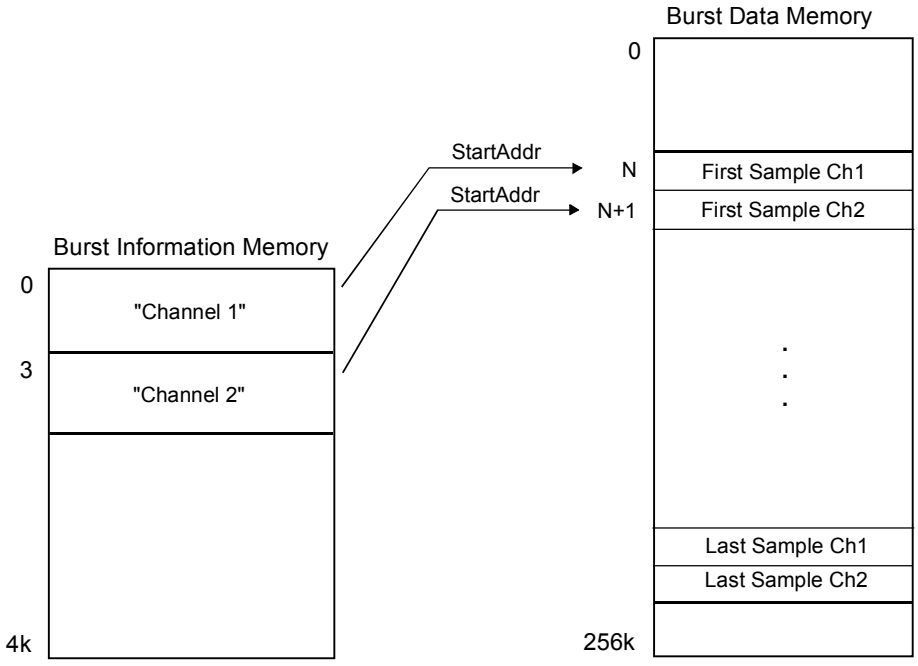
5.3.4 Data Structure / Memory Segmentation:

Exactly one segment has to be defined for each Burst Data Memory. Despite this limitation there is still the possibility to define the start address and the length of the segment for each Burst Data Memory separately. The software cannot change these settings during a running burst. Different settings are required for the Reload Mode with only one channel selected and both channels selected.

One channel: The structure of the data in the Burst Information Memories and the Burst Data Memories are the same as for the Memory Extension Mode unless the maximum numbers of segments is one.

Resource	Value
C1SegNo register	0
C2SegNo register	0

Two channels: The data for both channels are stored in the Burst Data Memory in a multiplexed way. This means each sample for channel 1 is followed by a sample for channel 2. Despite the fact that the internal circuitry considers each Burst Data Memory as one segment, two segments have to be defined in the Burst Information memory. The first segment describes the address of the first sample and the numbers of samples of channel 1. The second segment describes the address of the first sample and the numbers of samples of channel 2.



Resource	Value
C1SegNo register	0
C2SegNo register	0
Start Address of channel 2	Start Address of "channel 1" + 1
Length of channel 2	Length of channel 1

5.3.5 Burst Start

A burst cannot be started until the burst generation has been enabled by setting the Burst Start bit in the FCCSR register. This bit has to be set the whole time while the burst is running. Accesses to the resources mentioned in the FCCSR register description are disabled after the Burst Start bit is set.
The burst can be started either by a Software trigger or an external trigger. The first sample will be generated with the selected Burst Delay Time after the trigger occurred.

Software trigger: The software can start the burst generation by setting the Soft Trig bit in the FCCSR register. This bit will be cleared automatically after the burst is finished. The start by the software is always possible, even if the external trigger is enabled.

External trigger: The software must set the Ext Trig Enable bit in the FCCSR register to allow the burst start by an external trigger. The trigger can come from the Front Panel and / or the motherboard. For further information see the TrgInConf register and Burst Control by External Trigger.

5.3.5.1 Burst Break

There is the possibility to interrupt a running burst. This is called Burst Break and can be achieved by a software command or an external trigger. After receiving an event the burst stops and the DACs keep the last value written to it. The burst resumes with the next sample after clearing the event.

Software break: Setting the Soft Break bit in the FCCSR registers interrupts the burst. The burst stays interrupted until the software clears the Soft Break bit. The burst continues with the next sample after clearing the bit. The break by the software is always possible, even if the external trigger is enabled.

External trigger: The software must set the Ext Trig Enable bit in the FCCSR register to allow the burst break by an external trigger. The trigger can come from the Front Panel and / or the motherboard. For further information see the TrgInConf register and Burst Control by External Trigger.

5.3.6 Burst Stop

A running burst can be stopped either by a software command or by an external trigger. This function is especially important for the continuous waveform or burst mode because it is the only possible way to finish the burst operation in these modes.
Normally the burst will be stopped immediately after receiving the event. The stop can be synchronized with the end of the current pattern. Set the Sync Abort bit in the FCCSR register to select this stop mode.

Software abort: Setting the Soft Abort bit in the FCCSR registers stops the burst. The stop by the software is always possible, even if the external trigger is enabled.

External trigger: The software must set the Ext Trig Enable bit in the FCCSR register to allow the burst stop by an external trigger. The trigger can come from the Front Panel and / or the motherboard. For further information see the TrgInConf register and Burst Control by External Trigger.

5.3.7 Burst Control by External Trigger

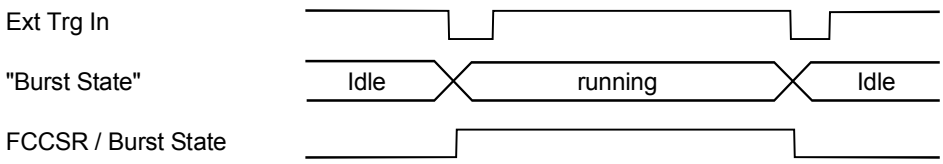
There is the possibility to control the burst generation by applying external triggers. The external trigger can come either from the Front panel and / or the motherboard. This selection is made in the TrgInConf register by setting the corresponding bits (FP In En, MB In En).
Note: There is an additional enable bit for the external trigger inputs in the FCCSR register (Ext Trig Enable). This bit works as a global enable.
The active level for the external trigger inputs is low. This means the internal logic reacts on the falling edge or the low level of the enable trigger input depending on the mode (Pulse Mode or Gate Mode).
Note: The burst control by software is always possible, even if the external trigger is enabled.

- **Pulse Mode**

  To select the Pulse Mode set the Mode bit in the TrgInfConf to zero (0).
  The burst will be started with the first falling edge on the external trigger, after the burst generation has been enabled (FCCSR / Burst Start = 1) and the burst is not started yet (FCCSR / Burst State = 0) by another event (e.g. Software trigger).
  The meaning of further trigger pulses is given by the setting of the Sub Mode bit in the TrgInConf register.

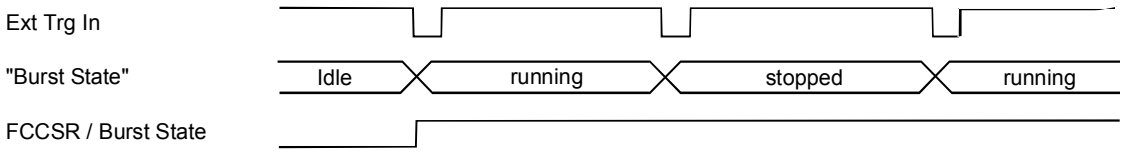
  - **Abort:** Sub Mode = 0

    If a falling edge on the external trigger occurs when the burst has been started and is still running (FCCSR / Burst State = 1), then the burst generation will be aborted (FCCSR / Burst State = 0).



  - **Break:** Sub Mode = 1

    If a falling edge on the external trigger occurs when the burst has been started and is still running (FCCSR / Burst State = 1), then the burst will be stopped and resumes with the next falling edge on the external trigger. This can be repeated as long as the burst is not Idle.

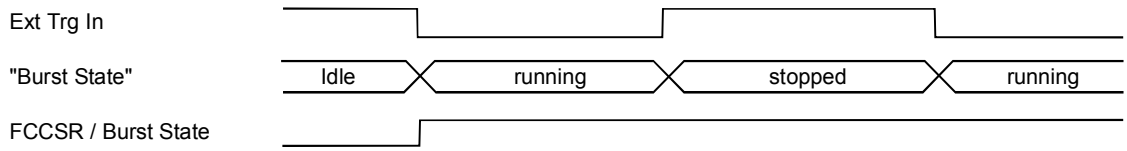


    Note: A burst running in either continuous waveform or continuous burst can not be aborted by external trigger if the Pulse / Break mode is selected.

- **Gate Mode**

  To select the Gate Mode set the Mode bit in the TrgInConf register to one (1).
  The burst will be started with a low level on one external trigger, after the burst generation has been enabled (FCCSR / Burst Start = 1) and the burst is not started yet (FCCSR / Burst State = 0) by another event (e.g. Software trigger).
  After the burst has been started, it keeps running as long as the external trigger is low and the burst end is not reached or a Software Abort command was sent.
  If the burst is still running and the external trigger goes high, then the burst will be stopped until the external trigger goes low again. This can be repeated as long as the burst is not Idle. The channel output stay at the last level before stopping the burst.

Note: If both external trigger sources are enabled (Motherboard, Front Panel), then both trigger sources have to be high to stop the burst.



5.3.8 Trigger Event Generation

The following events can be selected to announce several states of the burst generation. All settings for the trigger event generation have to be made in the Trigger Output Configuration register (TrgOutConf).

Description	Event	Enable bit (TrgOutConf)
Burst Start	First Sample of the Burst	Start Burst En
Burst End	Last Sample of the Burst	End Burst En
Waveform End	Last Sample of the Waveform	End Wave En
Pattern End	Last Sample of the Pattern	End Patt En
Segment End	Last Sample of the Segment (if enabled in the segment definition)	End Seg En

Note: There is an additional enable bit for the Segment End for each segment. This bit is located in the segment definition, which is given in the Burst Information Memory (see 3.4.2).

The event (trigger) can be routed to the Front panel and / or the motherboard by setting the corresponding enable bits (FP Out En, MB Out En). The trigger at the Front panel is always an active low pulse of 100ns width. The type of the trigger to the motherboard can be either a pulse or a level selected by the MB Out Type bit. The pulse is the same as at the Front panel. The level is active low and will be reset by reading the TrgOutConf register.

5.3.9 External Clock

One connection on the Front Panel provides the possibility to apply an external clock as update clock for the DACs. This clock goes to the programmable clock circuitry. Therefore there are all possibilities to generate different delay and update times according to the settings in the TBD, UPDTIME and TWD registers.
Note: The minimum setting for the TBD value is 2.
Set the Ext Clk Enable bit in the FCCSR register to select the external clock as base clock for the burst generation.
The following parameters apply in the relation between the external clock and the update clock due to the synchronization of the external clock with the internal clock.

Shift	max. Jitter
50ns	100ns

5.4 Filter and Calibration

5.4.1 Output Filter

Each channel is equipped with a 2-pole analog filter (Sallen-Key type) with three software-selectable cutoff frequencies. A filter bypass mode is also available. The filter setting for both channels can be made independently. For the settings see the FilterSel register.
In addition to the possible four cutoff frequencies and the bypass mode, the register can be used ground to the channel output. This does not effect the DAC register content and is the power-on state.
A different cutoff frequency can be selected during the calibration process. The original filter setting will be kept and restored automatically after the calibration is finished. The filter setting during the calibration is included in the Calib register.

5.4.2 Reference Voltage Setting

The circuitry for the automatic calibration uses onboard voltage references. The type of the voltage references depends on the function card subtype. The function card subtype is given at address 0 in the Serial PROM.

Subtype	pos. Voltage Reference	neg. Voltage Reference
+5V	+5V	-
+10V	+10V	-
+20V	+10V	-
± 5V	+5V	-5V
± 10V	+10V	-10V
± 20V	+10V	-10V

First adjustment or readjustment:
To adjust the voltage references, a value has to be written to the VoltRef register with the corresponding Select bit set. This value is typically around 800h for the positive voltage and C00h for the negative voltage. The output of the voltage reference should be checked using a highly precise DMM at the corresponding test points (TP501 = pos., TP502 = neg., TP503 = ground). The requested accuracy can be achieved by changing the register value in small steps.
The special adjustment software has to write the last register content (only Vref value) to the Serial PROM after finishing the adjustment by the operator.

Voltage Reference Value	Serial PROM Address
positive, MSB	1
positive, LSB	2
negative, MSB	3
negative, LSB	4

Adjustment after power-on / reset:
To adjust the voltage references after power-on, the driver software should perform the following 3 steps.

- Read the function card subtype from the Serial PROM address = 0
- Read the value of the pos. voltage reference from the Serial PROM address = 1 & 2 and write this value to the Vref register with Select = 0 (only in case of subtype bipolar or unipolar, pos.)
- Read the value of the neg. voltage reference from the Serial PROM address = 3 & 4 and write this value to the Vref register with Select = 1 (only in case of subtype bipolar or unipolar, neg.)

5.4.3 Offset Adjustment

To calibrate the offset of a channel, the software has to set the DAC first by writing the value 8000h to the DAC register. Writing to the Calib register starts the calibration. The following table shows the settings for the different function card subtypes.

Subtype	Calib type	FC type	DAC value
unipolar, positive	0	0	8000h
unipolar, negative	0	1	8000h
bipolar	0	0	8000h

The calibration for one channel takes approximately 1s and an error less than 1mV will be achieved. For detailed information of the calibration and its states see the Calib register. The Offset Adjustment always has to be done before the Gain Adjustment.

5.4.4 Gain Adjustment

To calibrate the gain of a channel, the software has to set the DAC first by writing the value 7FFFh to the DAC register. Writing to the Calib register starts the calibration. The following table shows the settings for the different function card subtypes.

Subtype	Calib type	FC type	DAC value
unipolar, positive	1	0	7FFFh
unipolar, negative	1	1	7FFFh
bipolar	1	0	7FFFh

The calibration for one channel takes approximately 1s and an error less than 1mV will be achieved. For detailed information of the calibration and its states see the Calib register. The Offset Adjustment always has to be done before the Gain Adjustment.

6. Front Panel Connector

The front panel is fitted with a high-density female 50-pin SCSI type connector or five female Lemo connectors.

6.1 Pin assignment of the SCSI connector:

Signal	A	B	Signal
DGND	1	26	TRG IN
DGND	2	27	DGND
DGND	3	28	DGND
DGND	4	29	DGND
DGND	5	30	DGND
DGND	6	31	DGND
DGND	7	32	EXT CLK
DGND	8	33	DGND
DGND	9	34	DGND
NC	10	35	NC
AGND	11	36	CH2
AGND	12	37	AGND
CH2	13	38	CH2
AGND	14	39	AGND
AGND	15	40	CH2
AGND	16	41	AGND
AGND	17	42	CH1
AGND	18	43	AGND
CH1	19	44	CH1
AGND	20	45	AGND
AGND	21	46	CH1
NC	22	47	NC
DGND	23	48	DGND
DGND	24	49	DGND
DGND	25	50	TRG OUT

NC: not connected

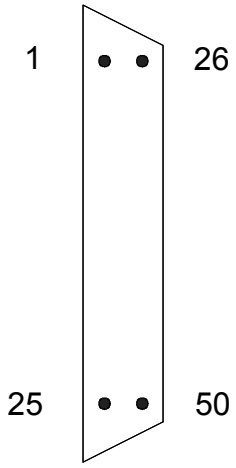


Fig. 3: Front panel connector pin assignment as seen when FDAC function card is fitted within a ProDAQ module in a VXI crate.

6.2 Pin assignment of the Lemo connectors:

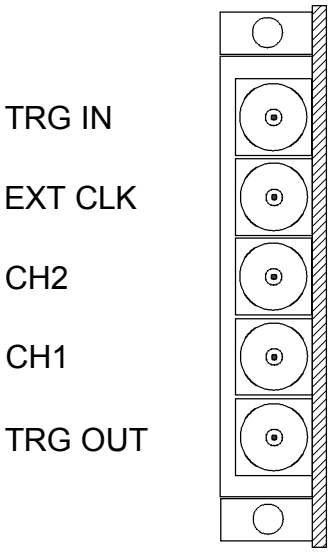


Fig. 4: Front panel connector pin assignment as seen when FDAC function card is fitted within a ProDAQ module in a VXI crate.

Note: Connector outside is always connected to Ground

⇒ Analog Ground for CH1 & 2

⇒ Digital Ground for TRG IN, TRG OUT & EXT CLK

7. Specifications

Number of Outputs	2
Output Voltage Range	0...5V, 0...10V, 0...20V, ±5V, ±10V, ±20V (other ranges available on request)
Resolution	16-bit
Total DC Error	max. ±0.01% for up to 10V FSR = ±1mV max. ±0.05% for up to 40V FSR = ±20mV
Output Update Time	DC to 1µs
Output Filter Type	2-pole Analog Filter (Sallen-Key type)
Filter Cutoff Frequency	100KHz, 10KHz, 1KHz, Bypass
Output Impedance	< 10mΩ
Output Coupling	DC
Output Current	±35mA
Internal Trigger	from motherboard, Clock divider
External Trigger	one input on the front-end SCSI connector or Lemo connector
Trigger Outputs	1 front panel or Lemo connector, TTL Open Collector with 1kΩ pullup
Power Requirements	12 mA @ +24V 12 mA @ -24V 26 mA @ +15V 20 mA @ -15V 76 mA @ +12V 66 mA @ -12V 250 mA @ +5V
Power Consumption	max. 3.9W
Warm-up Time	< 30 min
Operating Temperature	0°C to 50°C
Storage Temperature	-40 °to 70°C

Bustec Production, Ltd.
World Aviation Park, Shannon, Co. Clare, Ireland
Tel: +353 (0) 61 707100, FAX: +353 (0) 61 707106

Bustec, Inc.
17820 Englewood Dr #14, Middleburg Hts, OH 44130, U.S.A
Tel. +1 440 826 4156, Fax: +1 440 826 4184